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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,259	BUER ET AL.	
	Examiner	Art Unit	
	J. H. Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,13-17,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,13-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05 January 2009 has been entered.

Amendment

2. Acknowledgment is made of applicant's Amendment, filed 05 January 2009. The changes and remarks disclosed therein have been considered.

Claim 21 has been added by Amendment. Therefore, claims 1, 4-10, 13-17, 20 and 21 are pending in the application.

Specification

3. Claim 8 is objected to because of the following informalities:

In claim 8, the claim dependency appears to be in error; it will be understood to depend on claim 7 (instead of claim 1). Further, "both first and second" should be --both said first and second--, and "is equal to a first and second expected states" as --are respectively equal to first and second expected states--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-10, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,996,091 ("JONES") in view of U.S. Pat. No. 6,611,040 ("GELSOMINI").

Regarding claim 1, JONES, for example in Figs. 3a and 3b, discloses a method of verifying a state of an element (for example, an element of memory 304 in Fig. 3a corresponding to VERIFY DATA 0 in Fig. 3b) comprising: determining if the state of the element (VERIFY DATA 0 in Fig. 3b) is equal to an expected state (DR0 in Fig. 3b) using a verify circuit (308 in Fig. 3a; see also Fig. 3b); and outputting a valid signal (FAST VERIFY OUTPUT of 390 in Fig. 3b) if the state of the element is equal to said expected state (if VERIFY DATA 0 is equal to DR0 in Fig. 3b; see also column 4, lines 21-27).

JONES also implies that fuses (or antifuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in JONES (see for example column 13, lines 23-26).

JONES does not disclose that the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick and that the state of the element is a state of the electrical resistance of the element.

GELSOMINI discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (i.e., the state of the fuse/antifuse is determined by, or based on, the electrical resistance/conductivity of the fuse/antifuse, which is inherent for fuses/antifuses; see also column 7, lines 16-22).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the memory element of JONES with a thin oxide gated fuse of GELSOMINI having an oxide that is less than 2.5nm thick as an optimum thickness, as an equivalent memory element recognized in the art (JONES, column 13, lines 23-26), such that the state of the element (for example, VERIFY DATA 0 in Fig. 3B of JONES) would be determined by, or based on, a state of the electrical resistance of the element (as implied in, for example, GELSOMINI, column 7, lines 16-22), for the purpose of minimizing the voltage and duration of a programming pulse for the memory element (as implied in GELSOMINI, column 4, lines 2-6) with a reasonable expectation of success. Further, discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art (see MPEP 2144.05 I and II).

Regarding claims 4-8, the above combination further discloses sensing the state of the element (to obtain VERIFY DATA 0 in Fig. 3b of JONES, as applied to the above combination; see also sense amplifiers S/A 132 in Fig. 1 of GELSOMINI);

generating a high signal if the state of the element is equal to said expected state (the output of 390 in Fig. 3b of JONES, as applied to the above combination; see also JONES column 4, lines 21-27);

generating a low signal if the state of the element is not equal to said expected state (the output of 390 in Fig. 3b of JONES; see also column 4, lines 21-27);

wherein determining the state of the element includes determining states of first and second thin oxide gated fuses (for example, VERIFY DATA 0 and VERIFY DATA 9 in Fig. 3b of JONES, as applied to the above combination);

wherein outputting a valid signal includes determining if the states of the both first and second thin oxide gated fuses (for example, VERIFY DATA 0 and VERIFY DATA 9 in Fig. 3b of JONES, as applied to the above combination) are respectively equal to first and second expected states (for example, DR0 and DR9).

Regarding claim 9, JONES, for example in Figs. 3a and 3b, discloses a method for verifying a state of a memory device (304 in Fig. 3a) comprising: comparing a state of a first element (corresponding to VERIFY DATA 0 in Fig. 3b) to a first expected state (DR0 in Fig. 3b), and generating a first signal (output of 380); comparing a state of a second element (corresponding to VERIFY DATA 9 in Fig. 3b) to a second expected state (DR9 in Fig. 3b), and generating a second signal (output of 389); and outputting a valid signal (FAST VERIFY OUTPUT of 390) if both said first and second signals are the same (the XNOR function of 390).

JONES also implies that fuses (or antifuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in JONES (see for example column 13, lines 23-26).

JONES does not disclose that the first and second elements are thin oxide gated fuses having an oxide that is less than 2.5nm thick, and that the state is a state of the electrical resistance.

GELSOMINI discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (i.e., the state of the fuse/antifuse is determined by, or based on, the electrical resistance/ conductivity of the fuse/antifuse, which is inherent for fuses/antifuses; see also column 7, lines 16-22).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the memory element of JONES with a thin oxide gated fuse of GELSOMINI having an oxide that is less than 2.5nm thick as an optimum thickness, as an equivalent memory element recognized in the art (JONES, column 13, lines 23-26), such that the state of the element (for example, VERIFY DATA 0 in Fig. 3B of JONES) would be determined by, or based on, a state of the electrical resistance of the element (as implied in, for example, GELSOMINI, column 7, lines 16-22), for the purpose of minimizing the voltage and duration of a programming pulse for the memory element (as implied in GELSOMINI, column 4, lines 2-6) with a reasonable expectation of success. Further, discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art (see MPEP 2144.05 I and II).

Regarding claim 10, the above combination discloses the method of claim 9, with the exception of outputting a valid signal if both said first and second signals are high. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to output a valid signal if both said first and second signals are high (and modify accordingly the comparison logic of Fig. 3b of JONES; also compare, for example, Figs. 16a and 18a), since such designation of a logic state to indicate a result of a logic operation and a corresponding logic circuit modification require only routine skill in the art.

Regarding claims 13 and 14, the above combination further discloses determining if said state of said first thin oxide gated fuse is equal to said first expected state (via 380 in Fig. 3b of JONES, as applied to the above combination), and determining if said state of said second thin oxide gated fuse is equal to said second expected state (via 389 in Fig. 3b of JONES, as applied to the above combination).

Regarding claim 17, JONES, for example in Figs. 3a and 3b, discloses a method for verifying a state of a memory device (304 in Fig. 3a), comprising: setting a first expected state (DR0 in Fig. 3b); sensing a state of a first element (to obtain VERIFY DATA 0); determining if said state of said first element (VERIFY DATA 0) is equal to said first expected state (via 380) and generating a first signal (output of 380); setting a second expected state (DR9 in Fig. 3b); sensing a state of a second element (to obtain VERIFY DATA 9); determining if said state of said second element (VERIFY DATA 9) is equal to said second expected state (via 389) and

generating a second signal (output of 389); and generating a valid output (FAST VERIFY OUTPUT of 390) if both said first and second signals are the same (the XNOR function of 390).

JONES also implies that fuses (or antifuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in JONES (see for example column 13, lines 23-26).

JONES does not disclose that the first and second elements are a thin oxide gated fuse having an oxide that is less than 2.5nm thick, and that the state is a state of the electrical resistance.

GELSOMINI discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (i.e., the state of the fuse/antifuse is determined by, or based on, the electrical resistance/conductivity of the fuse/antifuse, which is inherent for fuses/antifuses; see also column 7, lines 16-22).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the memory element of JONES with a thin oxide gated fuse of GELSOMINI having an oxide that is less than 2.5nm thick as an optimum thickness, as an equivalent memory element recognized in the art (JONES, column 13, lines 23-26), such that the state of the element (for example, VERIFY DATA 0 in Fig. 3B of JONES) would be determined by, or based on, a state of the electrical resistance of the element (as implied in, for example, GELSOMINI, column 7, lines 16-22), for the purpose of minimizing the voltage and duration of a programming pulse for the memory element (as implied in GELSOMINI, column 4, lines 2-6) with a reasonable expectation of success. Further,

discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art (see MPEP 2144.05 I and II).

6. Claims 15, 16, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,996,091 ("JONES") in view of U.S. Pat. No. 6,611,040 ("GELSOMINI") as applied to claims 1 and 9 above, and further in view of U.S. Pat. No. 5,384,746 ("GIOLMA").

Regarding claims 15, 16 and 21, the above combination discloses the methods of claims 1 and 9, but does not disclose mirroring and comparing reference and fuse currents, or that the verify circuit comprises a current amplifier. GIOLMA discloses a current amplifier sensing means (12 in Fig. 1) including mirroring and comparing reference and fuse currents (see for example Fig. 1 and column 1, lines 50-65; see also column 3, line 17 through column 4, line 25). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate a current amplifier sensing means including mirroring and comparing reference and fuse currents (similar to that of GIOLMA) in the methods of the above combination (for example, to obtain VERIFY DATA 0 in Fig. 3b of JONES, in the above combination), for the purpose of preventing a false reading of a data fuse (see for example GIOLMA, column 1, lines 66-68).

Regarding claim 20, JONES, for example in Figs. 3a and 3b, discloses a memory device comprising: at least one memory cell (within 304 in Fig. 3a); at least one verify circuit (308) connected to said memory cell; sensing a state of said at least one memory cell (to obtain

VERIFY DATA 0 in Fig. 3b); at least one exclusive nor gate (390 in Fig. 3b) connected to said verify circuit; and a logic gate (380) connected to said exclusive nor gate generating a valid signal (see Fig. 3b).

JONES also implies that fuses (or antifuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in JONES (see for example column 13, lines 23-26).

JONES does not disclose at least one reference cell; and that the at least one memory cell has at least one thin oxide gated fuse having an oxide that is less than 2.5nm thick, and that the state is a state of the electrical resistance.

GELSOMINI discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (i.e., the state of the fuse/antifuse is determined by, or based on, the electrical resistance/ conductivity of the fuse/antifuse, which is inherent for fuses/antifuses; see also column 7, lines 16-22).

GIOLMA discloses a sensing means (for example, 12 in Fig. 1) including a reference cell (22).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the memory element of JONES with a thin oxide gated fuse of GELSOMINI having an oxide that is less than 2.5nm thick as an optimum thickness, as an equivalent memory element recognized in the art (JONES, column 13, lines 23-26), such that the state of the element (for example, VERIFY DATA 0 in Fig. 3B of JONES) would be determined by, or based on, a state of the electrical resistance of the element (as

implied in, for example, GELSOMINI, column 7, lines 16-22), for the purpose of minimizing the voltage and duration of a programming pulse for the memory element (as implied in GELSOMINI, column 4, lines 2-6) with a reasonable expectation of success. Further, discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art (see MPEP 2144.05 I and II).

In addition, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate a sensing means including at least one reference cell (similar to that of GIOLMA) in the memory device of the above combination (for example, to obtain VERIFY DATA 0 in Fig. 3b of JONES, in the above combination), for the purpose of preventing a false reading of a data fuse (see for example GIOLMA, column 1, lines 66-68).

Response to Arguments

7. Applicant's arguments filed 05 January 2009 have been fully considered but they are not persuasive.

Applicant primarily argues, at the bottom of page 5 through the top of page 6, that "[w]hile XOR gates measure signals - XOR gates do not electrical resistance."

In response, firstly, the argument is understood to be referring to XOR gates operating with logic signals; secondly, when GELSOMINI's fuse/antifuse is substituted for the memory element in the JONES/GELSOMINI combination, in obtaining the VERIFY DATA 0 signal in Fig. 3b of JONES, although it may be a logic signal, it is inherently determined by, or based on, a state of the electrical resistance/conductivity of the fuse/antifuse.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. H. Hur whose telephone number is (571)272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. H. Hur/ 3/26/2009
Primary Patent Examiner, Art Unit 2824